claims, applicants have amended independent claim 1 to recite the features of allowable claim 5, which should place claim 1 in condition for immediate allowance.

Claim 12 recites a method of manufacturing a system semiconductor device, with such method comprising a first step of fabricating a system LSI cell portion, a second step of fabricating a global wiring layer separate from the fabricated system LSI cell portion, and a final step of laminating the system LSI cell portion with the separately fabricated global wiring layer.

The applied YAMAZAKI et al. reference describes a semiconductor integrated circuit device having a multiple layer structure as illustrated generally in Figure 5B thereof. The description provided throughout the narrative portion of the applied reference describes only the structure of the disclosed circuit, without any consideration given to a method by which it is formed. Therefore, the applied reference necessarily fails to anticipate any method, including the method recited in rejected claim 12. This is even more clearly the case in light of the recitations of amended independent claim 12, which explicitly requires fabrication of a global wiring layer separate from the fabricated system LSI cell portion, followed by lamination of the two separately formed elements with one another.

This characteristic of the present invention is evident from the description of the disclosed method beginning on page 9,

a

line 7 of the present application. The description of the method of fabricating the system LSI cell portion begins on page 9, line 9 and continues to page 10, line 3, in correspondence with Figures 4A-4C. The description of the method step of fabricating the global wiring layer begins immediately thereafter in connection with Figures 5A-5F.

As is evident from these passages and the corresponding figures, the system LSI cell portion and the global wiring layer are fabricated entirely separately from one another. As described beginning on page 11, line 14 in connection with Figures 6A-6C, the final step is laminating the separately formed system LSI cell portion and global wiring layer.

These characteristics of the present invention are now clearly manifest in amended claim 12. As the applied reference clearly fails to disclose the method of claim 12, applicants respectfully suggest that the present anticipation rejection cannot be maintained.

The Official Action rejects claims 2-4, 7-11, 13-15, and 18-22 under 35 USC §103(a) as being unpatentable over YAMAZAKI et al. Reconsideration and withdrawal of this rejection are respectfully requested for the following reasons:

Applicants have canceled claims 3 and 4, rendering the rejection of such claims moot. The remaining rejected claims that depend from independent claim 1 should be allowable at least by virtue of their dependence from claim 1 in its amended form.

Each of the remaining rejected claims depends directly from amended independent method claim 12. As discussed above in connection with the anticipation rejection, amended claim 12 recites separate fabrication of the system LSI cell portion and the global wiring layer, as well as the subsequent lamination of the two separately fabricated elements with one another.

The applied reference provides no teaching or suggestion whatsoever as to a method for fabricating the semiconductor integrated circuit device disclosed therein. Therefore, neither this nor any other identified reference teaches or suggests the inventive method recited in the rejected claims at least by virtue of their dependence from amended independent claim 12.

For these reasons, applicants respectfully suggest that the applied reference fails to teach or suggest the full set of features recited in the rejected claims, and as a consequence suggest the present obviousness rejection cannot be maintained.

The Official Action explicitly states that claims 5, 6, 16, and 17 are allowable but for their dependence from rejected base claims. Please note that applicants have amended each of the allowable claims into independent form. These claims should therefore be in condition for immediate allowance regardless of the disposition of original independent claim 12.

Applicants have also added new claim 23. This claim depends from claim 1 and recites further features neither disclosed, taught, nor suggested by the applied reference.

a

In light of the amendments described above and the arguments offered in support thereof, applicants believe that the present application is in condition for allowance and an early indication of the same is respectfully requested.

If the Examiner has any questions or requires further clarification of any of the above points, the Examiner may contact the undersigned attorney so that this application may continue to be expeditiously advanced.

Attached hereto is a marked-up version of the changes made to the claims. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

YOUNG & THOMPSON

By _____

Eric Jensen
Attorney for Applicants
Registration No. 37,855
745 South 23rd Street
Arlington, VA 22202
Telephone: 521-2297

March 25, 2002

a

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 1 has been amended as follows:

--1. (amended) A system semiconductor device, comprising:

a system LSI cell portion which includes a plurality of functional blocks for realizing specific functions, each of the functional blocks serving as a unit circuit and being arranged on a semiconductor chip; and

a global wiring layer which has a wiring layer on a semiconductor substrate and which is laminated with the system LSI cell portion such that the functional blocks are electrically connected to each other;

wherein:

the global wiring layer comprises:

a first wiring layer formed on the semiconductor substrate,

an insulating layer formed on the first wiring layer,

a second wiring layer formed on the insulating layer, and

inner bumps formed on the second wiring layer.--

Claim 6 has been amended as follows:

--6. (amended) A system semiconductor device [claimed in claim 1,] comprising:

a system LSI cell portion which includes a plurality of

functional blocks for realizing specific functions, each of the functional blocks serving as a unit circuit and being arranged on a semiconductor chip; and

a global wiring layer which has a wiring layer on a semiconductor substrate and which is laminated with the system LSI cell portion such that the functional blocks are electrically connected to each other, wherein:

the global wiring layer comprises;

a first wiring layer formed on an organic substrate,

an insulating layer formed on the first wiring layer,

a second wiring layer formed on the insulating layer, and

inner bumps formed on the second wiring layer.--

Claim 7 has been amended as follows:

--7. (amended) A system semiconductor device as claimed in claim [3] 1, wherein[;] the insulating layer includes a via which electrically connects the first wiring layer with the second wiring layer.--

Claim 11 has been amended as follows:

--11. (amended) A system semiconductor device as claimed in claim [3] 1, wherein[:] the global wiring layer has at least one or more of the insulating layers.--

Claim 12 has been amended as follows:

--12. (amended) A method of manufacturing a system

a

semiconductor device, comprising the steps of:

fabricating a system LSI cell portion by forming a plurality of functional blocks which are constructed to serve as unit circuits and realize specific functions on a semiconductor chip,

fabricating a global wiring layer separate from the fabricated system LSI cell portion by forming a wiring layer on a semiconductor substrate, and

laminating the system LSI cell portion with the separately fabricated global wiring layer such that the functional blocks are electrically connected to each other.--

Claim 16 has been amended as follows:

--16. (amended) [A method as claimed in claim 12,] A method of manufacturing a system semiconductor device, comprising the steps of:

fabricating a system LSI cell portion by forming a plurality of functional blocks which serve as unit circuits and realize specific functions on a semiconductor chip,

fabricating a global wiring layer by forming a wiring layer on a semiconductor substrate, and

laminating the system LSI cell portion with the global wiring layer such that the functional blocks are electrically connected to each other;

wherein[:] the global wiring layer is formed by sequentially laminating a first wiring layer, a second wiring

a

layer, an insulating layer, and inner bumps on the semiconductor substrate.--

Claim 17 has been amended as follows:

--17. (amended) [A method as claimed in claim 12,] A method of manufacturing a system semiconductor device, comprising the steps of:

fabricating a system LSI cell portion by forming a plurality of functional blocks which serve as unit circuits and realize specific functions on a semiconductor chip,

fabricating a global wiring layer by forming a wiring layer on a semiconductor substrate, and

laminating the system LSI cell portion with the global wiring layer such that the functional blocks are electrically connected to each other;

wherein[:] the global wiring layer is formed by sequentially laminating a first wiring layer, an insulating layer, a second wiring layer, and inner bumps on an organic substrate.--

a